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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
COLEMAN, ERIC	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,836	HANSEN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/27/07, 2/28/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 recites the limitation "at least some of **the instructions** " in line 15 (as lines are number by applicant) . There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-22, are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22, of copending Application No. 10/757851. Although the conflicting claims are not identical,

they are not patentably distinct from each other because the features in the claims of instant application are included in the claims of patent No. 10/757851 as shown side by side below.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Application SN 10/757851	Application SN 10/757836 (Instant Application)
1. A method for processing data in a programmable processor, the method comprising: decoding and executing instructions that instruct a computer system to perform operations	1.A programmable processor comprising: an instruction path; a data path;an external interface operable to receive data from an external source and communicate the received data over the data path; a cache operable to retain data communicated between the external interface and the data path; a register file operable t receive to store from the data path and communicate the stored data to the data path; and a execution unit coupled to the instruction and data paths and operable to decode and execute instructions received from the instruction path

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at least some of the instructions including a group floating-point instructions each operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands; at least one group floating point instruction group floating-point multiply-add instruction, further operating on a third partitioned into a plurality of floating-point operands, operable to multiply the plurality of floating point operands in the first and second registers and add the plurality of floating point operands in the third register, each producing a floating point value to provide a plurality of floating point values, each of the floating point values capable of being represented by	, at least some of the instructions including a group floating point instruction, Operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands; at least some group floating-point instruction being a group floating-point multiply-and-add instruction further operating on a third register partitioned into a plurality of floating point operands, the execution unit operable to multiply a plurality of the operands in the first and second registers and add the plurality of floating point operands in the first and second registers and add the plurality of floating point operands in the third register, each producing a floating point value to

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the defined result precision, and a catenated result having a plurality of partitioned fields for the plurality of floating point values.	provide a plurality of floating point values, each of the floating point values capable of being represented by the defined result precision, and a concatenated result having a plurality of partitioned fields for receiving the plurality of floating point values.
2. The method of claim 1, wherein at least one group floating-point instruction being a member of the collection consisting of group floating point subtract, group floating point multiply, operable to perform subtract add, or multiply respectively on the plurality of floating point operands in the first and second registers to provide a plurality of floating point values, each of the floating point values capable of being represented by the defined result precision , and a catenated result having a plurality of	2. The system of claim 1, at least some of group floating-point instruction being at least one member of the collection consisting of group floating point subtract, group floating point add, and group floating point multiply, operable to perform subtract, add, and multiply respectively on the plurality of floating point operands in the first and second registers, each producing a floating point value to provide a plurality of floating point values, each of the floating point values capable of being represented by the defined result precision, and a catenated result having a

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partitioned fields for the plurality of floating point values; and at least one group floating point instruction being a member of the collection consisting of group floating-point set less, and group floating-point set greater of equal, operable to perform a	plurality of partitioned fields for receiving the plurality of floating point values; and at least some group floating point instruction being at least one member of the collection consisting of group floating point set less, and group floating point set greater or equal, operable to perform a
set-less or set-greater-or equal operation, respectively, on the plurality of floating point operands in the first and second registers to provide a plurality of values, each of the values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for the plurality of values, wherein the value is zero if the operation produces a false result, at least one of the instructions comprising performing data manipulations on multiple operands stored in partitioned fields of registers wherein the data	set-less and set greater or equal operation, respectively on the plurality of floating point operands in the first and second registers, each producing a value to provide a plurality of values, each of the values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of values, wherein the value is zero if the operation produces a false result, and wherein the value is an identity value if the operation produces a true result; and at least some of the instructions

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manipulations comprise copying or rearranging operands.	comprising performing data manipulations on multiple operands stored in partitioned fields of registers wherein the data manipulations comprise copying and rearranging operands.
3. The method of claim 2, wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using a bitwise Boolean operation.	3. the processor of claim 2, wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using a bitwise Boolean operation.
4. The method of claim 1 wherein the catenated result has a width of 128 bits.	4. The processor of claim 1, wherein the catenated result has a width of 128 bits.
5. The method of claim 1 wherein the catenated result is provided to a register.	5. The processor of claim 1, wherein the catenated result is provided to a register
6. the method of claim 1 wherein the defined precision is 16 bits.	6. The processor of claim 1, wherein the defined precision is 16 bits.
7. The method of claim 1, wherein the defined precision is a format comprising a one sign bit, five exponent bits and ten significand bits.	7, The processor of claim 1, wherein the defined precision is a format comprising one sign bit, five exponent bits and ten significand bits.

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8. the method of claim 1, wherein the defined precision is 32 bits.	8. The processor of claim1 wherein the defined precision is 32 bits.
9. The method of claim 1, wherein the precision of the group floating point instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits.	9. The processor of claim 1, wherein the precision of the group floating point instructions is a format one sign bit, eight exponent bits and 23 significand bits.
10. The method of claim 1, wherein the defined precision is 64 bits.	10. The processor of claim 1 wherein the defined precision is 64 bits.
11. The method of claim 1, wherein the precision of the group floating point instructions is a format comprising one sign bit, eleven exponent bits, and 52 significand bits..	11. The processor of claim 1, wherein the precision of the group floating point instructions is a format comprising one sign bit , eleven exponent bits and 52 significand bits.
12. A computer readable storage medium having stored therein a plurality of instructions that cause a computer processor to perform data operations:	12.A data processing system comprising (a) a bus coupling components in the data processing system; (b) an external memory coupled to the bus; (c) a programmable microprocessor coupled to the bus and capable of operation

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	independent of another host processor, the microprocessor comprising: a virtual
at least some of the instructions including group floating-point instructions each operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined	memory addressing unit ; an instruction and data path; an external interface operable to receive data from an external source and communicate the received data over the data path; cache operable to retain data communicated between the external interface and the data path; at least one register file configurable to receive and store data from the data path and to communicate the stored data to the data path; and at least some of the instructions including operating on first and second registers partitioned A group floating point instruction into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision

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precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands; the group floating point instruction including a group floating-point multiply-add instruction, further operating on a third partitioned into a plurality of floating-point operands, The group floating point multiply-and-add instruction operable to multiply the plurality of floating point operands in the first and second registers and add the plurality of floating point operands in the third register, each producing a floating point value to provide a plurality of floating point values, each of the floating point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for the plurality of floating point values.	which is equal to the defined precision of the operands; at least some group floating-point instruction being a group floating point multiply and add instruction, further operating on a third register partitioned into a plurality of floating point operands, the execution unit operable to multiply the plurality of floating point operands in the first and second registers and add the plurality of floating point operands in the third register each producing a floating point value to provide a plurality values capable of being represented by the defined result precision, and a concatenated result having a plurality of partitioned fields for receiving the plurality of floating point values.

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13. The computer-readable storage medium of claim 12, at least one group floating-point instruction being a member of the collection consisting of group floating point subtract, group floating point and add group floating point multiply, operable to perform subtract, add, or multiply respectively on the plurality of floating point operands in the first and second registers to provide a plurality of floating point values, each of the floating point values capable of being represented by the defined result precision , and a catenated result having a plurality of partitioned fields for the plurality of floating point values; and at least one group floating point instruction being a member of the collection consisting of group floating-point set less, and group floating-point set greater of equal, operable to	13. The system of claim 12, at least some of group floating-point instruction being at least one member of the collection consisting of group floating point subtract, group floating point add, and group floating point multiply, operable to perform subtract, add, and multiply respectively on the plurality of floating point operands in the first and second registers, each producing a floating point value to provide a plurality of floating point values, each of the floating point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values; and at least some group floating point instruction being at least one member of the collection consisting of group floating point set less, and group floating point set greater or equal, operable to perform a

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perform a set-less or set-greater-or equal operation, respectively, on the plurality of floating point operands in the first and second registers to provide a plurality of values, each of the values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for the plurality of values, wherein the value is zero if the operation produces a false result, at least one of the instructions comprising performing data manipulations on multiple operands stored in partitioned fields of registers wherein the data manipulations comprise copying or rearranging operands.	set-less and set greater or equal operation, respectively on the plurality of floating point operands i n the first and second registers, each producing a value to provide a plurality of values each of the values capable of being represented by the defined result precision, and catenated result having a plurality of partitioned fields for receiving the plurality of values, wherein the value is zero if the operation produces a false result, and wherein the value is an identity value if the operation produces a true result; and at least some of the instructions comprising performing data manipulations on multiple operands stored in partitioned fields wherein the data manipulations copying and rearranging operands.

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14. The computer-readable storage medium of claim 13, wherein the zero value are values that construct a bit mask operable to select alternate expressions using bitwise width of 128 bits.	14. the system of claim 13, wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using a bitwise Boolean operation
15, the computer readable storage of claim 12, wherein the concatenated result has a width of 128 bits.	15.The system of claim 12, wherein the catenated result has a width of 128 bits.
16. The computer readable storage of claim 12, wherein the concatenated result is provided to a register	16. The system of claim 12, wherein the catenated result is provided to a register
17. The computer readable storage of claim 12, wherein the defined precision is 16 bits.	17. The system of claim 12, wherein the defined precision is 16 bits.
18, The computer readable storage of claim 12, wherein the defined precision is a format is a format comprising one sign bit, five exponent and ten significand bits.	18, The system of claim 12, wherein the defined precision is a format comprising one sign bit, five exponent bits and ten significand bits.
19. The computer readable storage of claim 12, wherein the defined precision is 32 bits.	19. The system of claim12 wherein the defined precision is 32 bits.

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20. The computer readable storage of claim 12, wherein the precision of the group floating-point instructions is a format comprising one sign bit, eight exponent bits and 23 signi3ficant bits.	20. The system of claim 12, wherein the precision of the group floating point instructions is a format one sign bit, eight exponent bits and 23 significant bits.
21, The computer readable storage of claim 12, wherein the defined precision is 64 bits.	21. The system of claim 12 wherein the defined precision is 64 bits.
22. The computer readable storage of claim 12, wherein the precision of the group floating point instructions is a format comprising one sign bit eleven exponent bits and 52, significand bit.	22. The system of claim 12, wherein the precision of the group floating point instructions is a format comprising one sign bit , eleven exponent bits and 52 significand bits.

As can be seen by the side by side showing of the claims in the instant application and the corresponding claims 1-22 in SN 10/757851 both sets of claims are directed toward the same invention even though the claims are not identical (note claims 1-22 of Patent 10/757851 has similar features to claims 1-22 of the instant application and correspondingly provide the features of claims 1-22). As to the differences, Claims 1 and 12 of the instant application claim a data path, instruction path, cache, external

memory and external interface. Claim 1 of SN 10/757851 claims processing instructions on operating data in partitioned registers. At the time of the claimed invention the use of separate paths for data and instructions (e.g., Harvard architecture) as well as a memory hierarchy that included an external memory and cache well known in the art.. The motivation for use of the these well known features would have been to provide more efficient access to data and instructions as the separate data and instruction path would reduce the time waiting for data or instructions over a system with a singular path. Also storing of the data expected to be used in a high speed cache and the data and or instructions not expected to be used in a current processing in an external slower memory would have provided fast access to the instructions and data to be used in a current processing which would reduce the system cost since providing all data and instructions to be used for processing in registers would be very costly. Further as to the virtual addressing unit of claim 12 of the instant application, the claims of SN 10757851 include access to partitioned data including plural operands in a register for operating on the partitioned data as operands and concatenating the results. One of ordinary skill would have been motivated to operate the required means to address the data as a means to address the individual operands which would constitute a type of virtual addressing. Note addressing the first or second, etc. operand of a register where the address of one of the plural operands within the register would be a virtual address and would be used with the address of the register.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC
/Eric Coleman/
Primary Examiner, Art Unit 2183